CBCS SCHEME

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15CS32

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Explain the working of N-channel MOSFET, with the help of neat diagram. **(08 Marks)**

b. What are applications of FET? **(04 Marks)**

c. What are the ideal characteristics of op-amp? **(04 Marks)**

OR

2 a. Explain the performance parameters of op-amp. **(08 Marks)**

b. Explain the relaxation oscillator, with the help of neat diagram. **(08 Marks)**

Module-2

3 a. Minimize the following Boolean function using K-map method,
$F(A, B, C, D) = \sum m(0, 2, 3, 8, 10, 11, 12, 14)$ **(06 Marks)**

b. Apply Quine Mc-Cluskey method to find the essential prime implicants for the Boolean expression,
$F(A,B,C,D) = \sum m(0,1,2,3,10,11,12,13,14,15)$ **(10 Marks)**

OR

4 a. Minimize the following Boolean function using K-map method.
$F(A,B,C,D) = \Pi M(0,1,2,3,4) + \sum d(5,7)$ **(06 Marks)**

b. What is Hazard? Explain its types with examples. **(10 Marks)**

Module-3

5 a. Implement the following function using 8 : 1 multiplexer
$F(A,B,C,D) = \sum m(1,2,5,7,8,10,11,13,14,15)$ **(06 Marks)**

b. Realize the following function using 3 : 8 decoder

(i) $F(A, B, C) = \sum m(1,3,4)$

(ii) $F(A, B, C) = \sum m(3,5,7)$ **(04 Marks)**

c. Design a priority encoder using the truth table. The order of priority for three inputs is $X_1 > X_2 > X_3$ **(06 Marks)**

Truth Table

Input				Output	
S	X_1	X_2	X_3	A	B
0	X	X	X	0	0
1	1	X	X	0	1
1	0	1	X	1	0
1	0	0	1	1	1
1	0	0	0	0	0

OR

6	a.	Design seven segment decoder using PLA.	(08 Marks)
	b.	Design Half adder and Full adder.	(08 Marks)

Module-4

7	a.	Explain Smith contact bounce circuit.	(08 Marks)
	b.	Give state transition diagram and characteristic equations for SR-FF and JK-FF.	(08 Marks)

OR

8	a.	With neat diagram, explain Ring and Johnson counter.	(08 Marks)
	b.	What is shift register? With neat diagram, explain 4-bit parallel in serial out shift registers.	(08 Marks)

Module-5

9	a.	Define counter. Design mod-8 up synchronous counter using JK-FF.	(12 Marks)
	b.	Write VHDL code for mod-8 up counter.	(04 Marks)

OR

10	a.	Explain the binary ladder with digital of 1000.	(06 Marks)
	b.	Explain with neat diagram, single slope A/D converters.	(10 Marks)

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